DESIGN OF A LOW DROP-OUT VOLTAGE REGULATOR USING VLSI

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ABSTRACT

A Low-Voltage Low-Dropout (LDO) Voltage Regulator is proposed that can operate with a very small Input-Output Differential Voltage with nm CMOS technology, thereby increasing Packing Density and allowing for new approaches to power management. The proposed LDO regulator was created using 90nm CMOS technology. The area and power loss can be reduced. Furthermore, a maximum output variation for a load transient was achieved, as was a maximum current efficiency. Using bipolar transistor technology or a complex circuit to achieve a high PSR at the expense of a high quiescent current is, however, unnecessary for a general-purpose switching regulator's post regulator. The Error Amplifier (EA) is a Simple Symmetric Operational Trans-Conductance Amplifier with a current splitting technique used to boost the gain. This also improves the LDO Regulator's closed-loop bandwidth. A Power Noise Cancellation Mechanism is formed in the EA's rail-to-rail output stage, reducing the size of the Power MOS transistor. This paper will go over the design of a low drop-out voltage regulator using VLSI.

Keywords: *Design; Low Drop-Out; Voltage Regulator; Input–Output; Error Amplifier; Power Noise; System-On-Chip; DC Converter; Capacitor; Stability.*

INTRODUCTION

In today's global village, the use of battery power devices has become pervasive and indispensable in almost every aspect of life. The cost and size of the design are reduced by reducing the number of battery cells. This may reduce quiescent current flow, increasing battery life. LDOs, which include the growing family of portable battery products, are being used in an increasing number of low voltage applications. Voltage regulators maintain a constant voltage supply rail under all loads. [1]

Most battery-powered handheld electronics use power-saving techniques to reduce power consumption. In the world of electronics, CMOS linear regulators with low dropout and low supply current are more advantageous. LDO regulators allow batteries to be used up to a certain limit, so they are now required power management ICs for devices such as mobile phones, digital cameras, and laptop PCs to have long battery life. There is an increasing demand for stable LDOs with high PSR (power supply rejection), low drop-out voltage, and low quiescent current for a wide range of load conditions.

A low-dropout regulator, also known as an LDO regulator, is a DC linear voltage regulator that can operate with a very small input-output differential voltage. A low dropout voltage has several

advantages, including a lower minimum operating voltage, higher efficiency operation, and lower heat dissipation. The growing demand for portable appliances highlights the importance of complete system-on-chip (SOC) design solutions with smaller footprints and lower operating voltages. [2]

Low-dropout regulators (LDOs) are one of the most common power supply modules used in noise sensitive analogue. And LDO are critical components of the SOC application. To provide a regulated power source for noise sensitive blocks, a switching pre-regulator is usually followed by a low dropout (LDO)regulator. Because of its simple architecture and fast-responding loop, it is the best candidate for implementing these post regulators. The design focuses on improving transient response and driving a large current. The proposed LDO regulators achieved a high PSR over a wide frequency range.

Increased demand for portable appliances highlights the importance of complete system-on-chip (SoC) design solutions with smaller sizes and lower operating voltages. In today's global village, battery-powered devices are ubiquitous and indispensable in almost every aspect of life. The goal is to reduce the number of battery cells needed to reduce cost and size while minimising quiescent current flow to extend battery life. Current efficiency is especially important in low load current conditions because low current efficiency or high current flow reduces battery life. Indeed, the growing trend towards total chip integration necessitates the inclusion of power supply circuits in every chip.

Furthermore, as products achieve or approach total chip integration, most designs find it necessary to include regulators and other power supply circuits. Low dropout regulators are suitable for a wide range of circuit applications, including automotive, portable, industrial, and medical applications. [3]

Low dropout voltage is required in the automotive industry during cold-crank conditions when the battery voltage can drop below 6V. For increased battery efficiency and longevity, the portable electronics market requires low voltage and low quiescent current flow. As a result, in order to maximise battery life, high current efficiency is required. Low voltage operation is also a result of process technology's shift towards higher packing densities.

Because of the emphasis on efficiency, low dropout (LDO) regulators have become the most popular class of linear regulators. However, this increase in efficiency comes at the expense of the regulator's stability. LDO regulators have a high output impedance, which, together with the load capacitance, creates a low frequency pole and reduces the overall phase margin.

It is necessary to increase the power consumption of portable electronic appliances, as well as to use low power and high performance LDO. To meet the aforementioned requirements, several advanced techniques for designing a high performance LDO with fast load transient response, high power supply rejection ratio, small inrush current, good load regulation, and precise over current protection are proposed and presented. Another critical specification in voltage regulator design is bandwidth. [4]

DESIGN CONSIDERATIONS

When designing a low dropout regulator, many factors must be taken into account. Reducing power consumption is always beneficial, especially with portable consumer electronics. Because less power is consumed, the device's battery lasts longer, requiring the user to charge the battery less frequently. The dropout voltage determines efficiency. The dropout voltage is defined as the difference between the unregulated supply voltage and the regulated output voltage. Lowering the dropout voltage reduces the required voltage of the unregulated power supply, lowering the regulator's power consumption.

A device that consumes less power has a smaller battery and is more portable. The portability of the regulator improves as the area is reduced. Devices with multiple voltage regulators benefit greatly from a voltage regulator design that requires less space, because in-house circuitry can be made smaller and easier to transport. Because of the small area, more devices can be fixed onto a single wafer, lowering manufacturing costs. [5]

Because of the continuous downscaling of the supply voltage and the inherently noisy environment of SoCs, low-dropout regulators (LDOs) are required in modern system-on-chips (SoCs). Because the LDO is an analogue block, designing it is a difficult task that involves many trade-offs, design variables, and degrees of freedom. It is difficult to find a design point that meets all of the specifications.

There have been several attempts to automate or optimise the design of LDOs. An equation-based optimisation scheme is used in this case. The design equations are derived using a surrogate model for the LDO. To approximate the small signal behaviour of transistors, physics-based models and curve fitting are used. Although quick, this method lacks accuracy due to approximations in the equations and device models. [6]

LDO REGULATOR

Low dropout regulators can be classified as either low power or high power. The maximum output current of a low power LDO voltage regulator is less than 1A, making them suitable for portable applications. High power LDO voltage regulators provide currents equal to or greater than 1A and are used in automotive and industrial applications.

The LDO voltage regulator can produce regulated voltage with a very low dropout voltage. A low dropout regulator is a circuit that provides direct current voltage regulation even when the difference between the input and output voltages is very small. The minimum voltage required across the regulator to maintain regulation is defined as the dropout voltage. [7]

REVIEW OF LITERATURE

Chung-Hsun Huang (2013) stated in their paper "Design of a Low-Voltage Low-Drop-Out Regulator" that a low-voltage low-dropout (LDO) regulator converted a 1 V input to a 0.85-0.5 V output using

90-nm CMOS technology. Up until 2013, the current technology was in the higher range of nm technology. As a result, with the advancement of future technology in mind, the proposed project has been decided to focus on the selection of lower order nm technology. [8]

In Jayanthi Vanama's (2013) paper, "Design of a programmable low power low drop-out regulator," they created a low power low drop-out regulator that could deliver four different output voltages based on the control signals it received. The design achieves a gain of 30 dB, but an increase in differential pair transconductance can achieve a gain of up to 50 dB. The design suffered from an input offset disadvantage, as the input offset error can reach 10 mV. A folded cascade topology with resistive biassing can also generate more gain, reducing the number of stages and making the system's phase margin easier to achieve at lower values of external capacitance. [9]

OBJECTIVES

- Accurate supply voltage
- Active noise filtering
- Overcurrent protection
- Inter-stage isolation (decoupling)
- Multiple output voltage generation from a single source
- Useful in constant current sources

RESEARCH METHODOLOGY

This study's overall design was exploratory. This project's methodology is to improve the performance of low drop-out regulators for battery-powered electronics. This is intended to meet both current commercial requirements and projected future demands. To design a low-dropout (LDO) voltage regulator that can operate with a very small input-output differential voltage with 45nm CMOS technology, providing for new approaches to power management is proposed. [10]

The designed LDO is suitable for powering up low-voltage CMOS mixed-signal systems that require high precision supply voltage as well as low recovery speed.

RESULT AND DISCUSSION

The Low Drop-Out Voltage Regulator (LDO) is a critical module in CMOS design that provides regulated voltage to all analogue circuits connected to the LDO's load. This research paper focuses on the development of a reduced area LDO and Pass transistor circuit, as well as an output capacitor free LDO for advanced CMOS chip power control.

The 90nm CMOS technology on cadence will enable new approaches to power control. Power management is critical for all portable devices because it improves battery quality and runtime. As a result, selecting a suitable technique is a critical aspect for these devices. Power management modules

other than LDO include switching mode DC-DC converters and charge pumps. In many practical realisations, switching mode regulators provide efficiencies of more than 90%. [11]

However, switching regulator output ripple and noise may be unacceptable for critical radio frequency applications. Linear regulators have low output noise, a small output voltage ripple, and are stable with varying loads. Unfortunately, the efficiency of linear regulators is dependent on the dropout voltage. In most applications, a switching regulator is cascaded with a linear regulator to reduce voltage ripple and improve overall system stability. The LDO Voltage Regulator is a critical module that provides low noise and dc ripple voltages. The supply voltage for the System-on-Chip is generated by an external voltage source, as shown in the LDO block diagram below. [12]

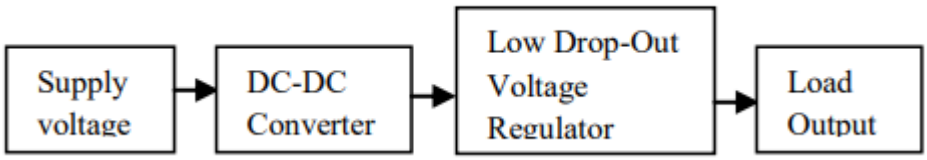

Figure 1: Block diagram of Low Drop-Out Voltage Regulator

Low-dropout (LDO) regulators work in the same way that all linear voltage regulators do. The primary distinction between LDO regulators and non-LDO regulators is their schematic topology. Low-dropout regulators use an open collector or open drain topology instead of an emitter follower topology, allowing the transistor to be easily driven into saturation with the voltages available to the regulator. This allows the voltage drop from unregulated to regulated to be as low as (limited to) the saturation voltage across the transistor. [13]

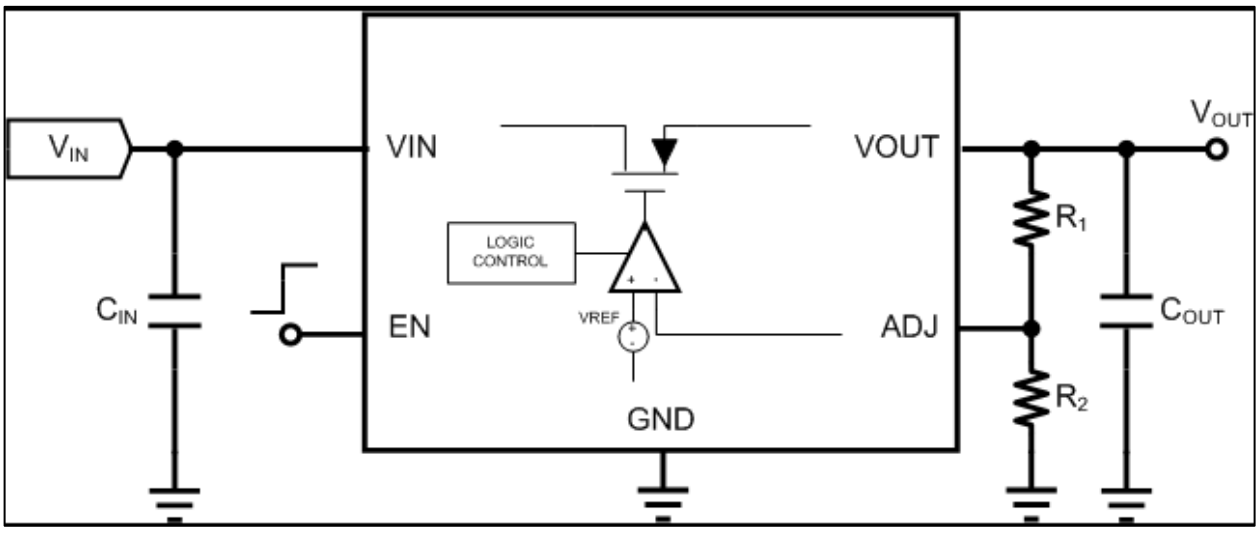

Figure 2: Schematic of a low-dropout regulator

The output voltage for the circuit shown in the figure to the right is:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

When a bipolar transistor is used instead of a field-effect transistor or JFET to control it, significant additional power may be lost, whereas non-LDO regulators take that power from the voltage drop itself.

There will be significant power loss in the control circuit for high voltages with very low In-Out difference. Because the power control element is an inverter, it requires another inverting amplifier to control it, increasing schematic complexity when compared to a simple linear regulator.

A voltage reference, an error amplifier, a feedback voltage divider, and a series pass element, usually a bipolar or CMOS transistor, comprise a low dropout regulator (LDO) (see Figure).

The error amplifier controls the output current, which is controlled by the PMOS transistor. If the feedback voltage is less than the reference voltage, the PMOS device's gate is pulled lower, allowing more current to pass and raising the output voltage.

If the feedback voltage exceeds the reference voltage, the PMOS device's gate is pulled higher, allowing less current to pass and decreasing the output voltage. The internal pole of the error amplifier/pass transistor and the external pole of the output capacitor's equivalent series resistance (ESR) form the basis of this closed-loop system.

Analogue Electronics When the recommended capacitors are used, LDOs are designed to be stable over the specified operating temperature and voltage ranges. The output capacitor's ESR influences the stability of the LDO control loop. To ensure stability, an ESR of 1 or less is recommended.

The transient response of LDOs to rapid changes in load current is also affected by output capacitance. Increasing the value of the output capacitor improves the LDO's transient response; however, it increases the start-up time. [14]

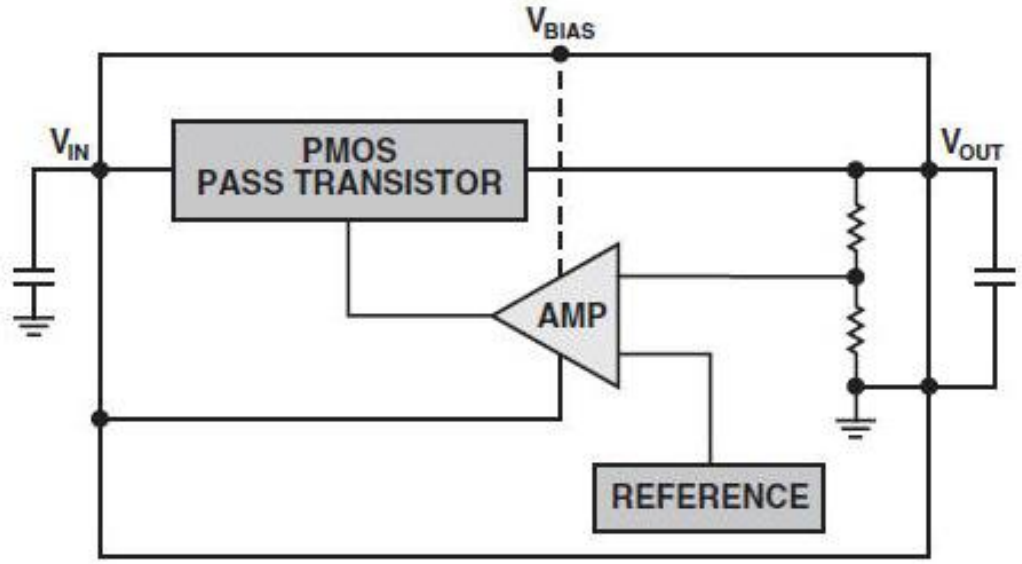

Figure 3: An LDO provides the required output voltage regulation from an input voltage with a low dropout (i.e., small difference between V_{IN} and V_{OUT})

Microwind3.1 VLSI Backend software is used in this design. This software allows for the physical description of an integrated circuit to be designed and simulated. The proposed LDO is built with 32 nm CMOS/VLSI technology in microwind3.1 software, resulting in high speed performance at low power. This layout design is implemented with 5 NMOS and 6 PMOS BSIM4 transistors with optimal transistor dimensions and metal connections that adhere to the lambda-based rules of the micro wind 3.1 software.

In CMOS digital integrated circuits, power dissipation is a strong function of the power supply voltage. As a result, reducing VDD emerges as a very effective method of limiting power consumption. A 1 volt power supply VDD is used for the proposed LDO.

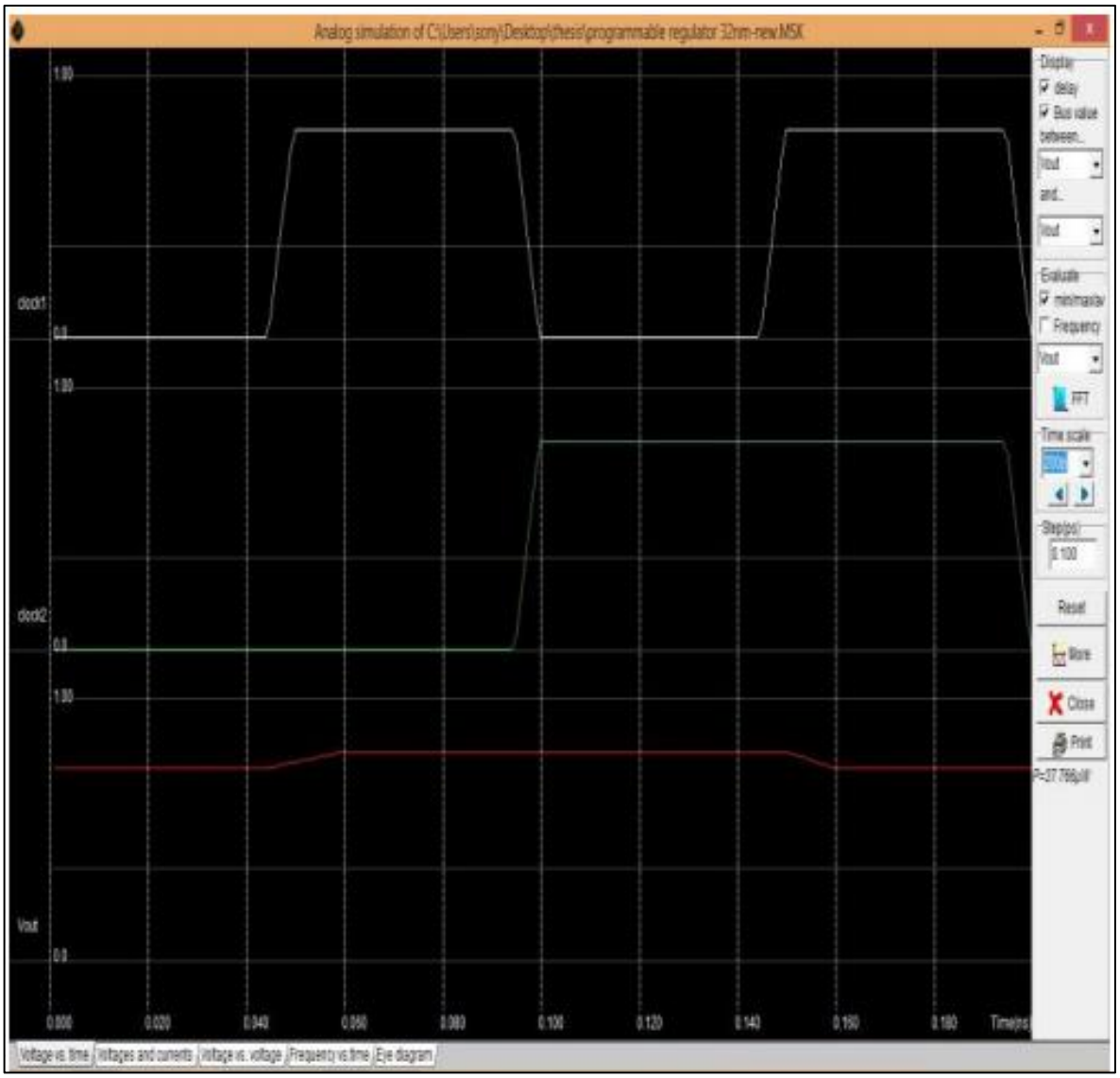

Figure 4: Regulated output of Programmable LDO Regulator [15]

Transient waveforms of a programmable LDO regulator are shown in Figure 4. When two external control signals are applied to the gate inputs of two NMOS transistors, the binary input that appears at the gate is responsible for bringing regulation into the circuit, and we get regulated programmable voltage for different levels, as shown in table 1.

This programmability enables two different output voltages for four control inputs with output-to-output dropout voltages as low as 60 mV and input-to-output dropout voltages as low as 200 mV.

It consumes 15.446w of power, which is extremely low. More than one application can benefit from programmability, which requires output voltage between 0.74V and 0.80V.

Table 1: Range of output voltages

Binary input	Output voltage
00	0.74
01	0.80
10	0.80
11	0.74

The programmable LDO has a width of 5.7m and a height of 2. 7m. Thus, the proposed Programmable LDO has a surface area of 15.2m2. There are 20 electrical nodes used. As a result, we used the fewest resources possible to achieve the best results.

Error Amplifier:

The error amplifier is a high gain operational amplifier with a stable voltage reference fed to one of its inputs. Typically, the voltage reference is derived from a bandgap reference circuit. The operational amplifier's differential pair is made up of a current mirror NMOS load and a PMOS tail current source, with the gate-drain connected load being driven by a 2.5 uA ideal current source.

A current mirror load has the advantage of having a high output impedance and, as a result, a high gain. With the exception of the differential pair, an operational amplifier connected to this type of load is referred to as an open-transconductance amplifier.

Design of Proposed LDO Regulator:

An EA, a power MOS transistor (Mp), a biassing circuit, and a feedback network comprise a basic LDO regulator. An off-chip output capacitor that is used to monitor output variation during a load transient. The difficulties and concepts of designing a low-voltage LDO regulator are discussed briefly below.

Input voltage and low quiescent current:

A high loop gain is required in the design of an LDO regulator to achieve optimal performance values such as accurate output and PSR. The achievable gain of the EA is limited by a low supply voltage and a reduction in output resistance caused by shrinking technology. An error amplifier with more than three stacked transistors between the supply voltage and ground is preferred for low-voltage operation.

Fast transient Response:

The voltage variation and recovery time during the load current transient are referred to as the transient response. The voltage variation is more important than the recovery time because even minor variations

in the output voltage can cause severe performance degradation in the load circuit operation. To reduce output voltage variation, both the LDO regulator's close loop bandwidth and the EA's output current slew rate must be large.

Power Supply:

Noise suppression is required to provide a clean and accurate output voltage with a low voltage level. With a low supply voltage, it is difficult to achieve a high loop gain.

Small area:

Several performance-enhancing auxiliary circuits and a large Mp take up a lot of space in a low voltage LDO regulator design. The Mp may enter the triode region to support a wide load current range and a wide output voltage range. Similarly, for such a wide range of operating conditions, the LDO regulator can respond to the load current transient in time.

Stability:

The output node contains the dominant pole for an off-chip capacitor compensated LDO regulator. [16]

CONCLUSION

We created a low-power, low-drop-out regulator that can deliver different output voltages based on the control signals. As a result, we were able to design an area efficient programmable low drop-out voltage regulator with very low power consumption, opening the door to extending the product's battery life.

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